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10/536,460	05/25/2005	Seiji Miura	XA-10365	6477

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/536,460	MIURA ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12,14-17,21,24,25,27,28 and 79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,14-17,21,24,25,27,28 and 79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 21 April 2008. Claims 1-10, 12, 14-17, 21, 24, 25, 27, 28 and 79 are pending. Claims 11, 13, 18-20, 22, 23, 26 and 29-78 are cancelled. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 12, 14, 21, 24, 25, 28 and 79 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiraki et al. [US 6,324,103 B2] (hereinafter "Hiraki").

Per claim 1, Hiraki teaches a memory module (see Figs. 1 and 20, Flash 11, DRAM 12 and SRAM 13 can be considered together as a memory module/section of the single chip microcomputer 1A, since the other major component, CPU 10 is not a memory) including a non-volatile memory (Flash 11), a dynamic random access memory (DRAM 12), a static random access memory (SRAM 12), and a control circuit that accesses the non-volatile memory, the dynamic random access memory, and the

static random access memory (see CPU 10 and all circuitry involved in repairing defects, see Figs 1, 14, 17 and 20), the memory module comprising:

a dynamic random access memory interface (Input Buffer 11IB, Output Buffer 11OB, Input Buffer 12IB and Output Buffer 12OB can be considered together as an interface since they interface Flash 11 with DRAM 12, and interface DRAM 12 with CPU 10) to outside the memory module for accessing the dynamic random access memory from outside the memory module (CPU 10 is outside of the memory module as described above; also see col. 10, lines 44-46); and

a static random access memory interface (Input Buffer 13IB, Output Buffer 13OB, Address Buffer 13AB and any other circuitry related to data transfer) to outside the memory module for accessing the static random access memory from outside the memory module (see col. 18, lines 28-43),

wherein the dynamic random access memory interface is arranged to connect to a first memory controller (see Fig. 1, Timing Controller 12TC and col. 17, lines 5-20 and the control logic/circuitry that provides functions such as activating the X decoder 12XD as a result of the Timing Controller 12TC detecting the operation select of the DRAM12), and

wherein the static random access memory interface is arranged to connect to a second memory controller, different from the first memory controller (see Fig. 1, Timing Controller 13TC and col. 18, lines 28-43 and the control logic/circuitry that provides functions such as activating the X decoder 13XD as a result of the Timing Controller 13TC detecting the operation select of the SRAM 13).

Per claim 2, Hiraki further teaches immediately after power is turned on (col. 13, lines 18-29 and Fig 3), data in a predetermined address region (col. 20, lines 41-45 and Fig.15) of the non-volatile memory is transferred to the static random access memory.

Per claim 3, Hiraki further teaches immediately after power is turned on (col. 13, line 18-29 and Fig 3), data in a predetermined address region (col. 20, lines 41-45 and Fig.15) of the non-volatile memory is transferred to the dynamic random access memory.

Per claim 4, Hiraki further teaches data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction sent via the dynamic random access memory interface ("Executing reading and setting operations", see col. 4, lines 1-10, col. 20, lines 57-67 and col.21, lines 1-3).

Per claim 5, Hiraki further teaches data transfer between the non-volatile memory and the static random access memory is performed according to an instruction sent via the static random access memory interface ("Executing reading and setting operations", see col. 4, lines 1-10, col. 20, lines 57-67 and col.21, lines 1-3).

Per claim 6, Hiraki further teaches in transferring data from the non-volatile memory to the static random access memory or the dynamic random access memory, data having an error is corrected before being transferred ("repair information", see col. 3, lines 25-67 and col. 4, lines 1-10; also see col. 21, lines 4-5, since the flash memory contains repair program and repair information, if itself contains defects then the defects on the flash memory needs to be corrected before transferred to the DRAM or SRAM for repair).

Per claim 7, Hiraki further teaches in transferring data from the static random access memory or the dynamic random access memory to the non-volatile memory, an address replacement process is executed ("repair address register", see Fig. 1, 14 and 17; "repairable redundancy construction" and "reprogramming the flash memory", see col. 12, lines 59-67, col. 13, lines 1-17, col. 14, 8-67 and col. 15, lines 1-22; it should be clear that when the repair program executing on the flash memory reads data from the DRAM and SRAM, the DRAM and SRAM must access the flash through their respective write and output buffers in order to provide the read information to the flash memory).

Per claim 8, Hiraki further teaches a boot program is held in the non-volatile memory (col. 3, lines 42-49, col. 6, lines 30-35 and 55-67, and col. 10, lines 25-35).

Per claim 9, Hiraki further teaches data transfer range data, which includes a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on, is held in the non-volatile memory (repairing defects on DRAM by transferring repair information from the flash memory after boot up/power on, see col. 14, lines 26-67 and col. 15, lines 1-22).

Per claim 12, Hiraki further teaches a data-hold operation of the dynamic random access memory is executed inside the memory module ("charge holding" and "data holding mode", see col. 24, lines 57-67 and col. 25, lines 1-47).

Per claim 14, Hiraki further teaches the memory module is accessed first (see col. 3, lines 53-60 and Fig. 1, Repair Address Register 12AR; DRAM must be accessed first for Repair Information to be stored in Repair Address Register 12AR which is part of DRAM12); the dynamic random access memory performs a data-hold operation second (see col. 3, lines 53-60 and Fig. 1, Repair Address Register 12AR, which holds Repair Information); the memory module performs data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory third (storing SRAM Repair Information onto SRAM 13 occurs after DRAM 12 has started to store and hold DRAM Repair Information, see the timing diagram in Fig. 18).

Per claim 21, Hiraki further teaches the dynamic random access memory includes with plural interfaces (Input Buffer 12IB, Output Buffer 12OB, Address Buffer 12AB, Repair Address Register 12AR; there are separate interfaces in DRAM 12 for control, address and data, see Fig. 1, 14, 17 and 20).

Per claim 24, Hiraki further teaches the dynamic random access memory includes a control circuit which processes access from outside of the memory module and a control circuit that independently (it should be clear the DRAM circuitry that handles the access performs its designed function independently since its own capabilities adequately performs the intended operations) accesses the non-volatile memory (see col. 17, lines 5-10, the DRAM circuitry to handle read/write accesses from the CPU 10; and it should be clear that when the repair program executing on the flash memory reads data from the DRAM, the DRAM must access the flash through its write and output buffers in order to provide the read information to the flash memory, see col. 16, lines 34-45 and col. 17, lines 9-16; also see Fig. 1, 14, 17 and 20 and "reprogramming the flash memory", see col. 14, lines 8-67 and col. 15, lines 1-22).

Per claim 25, Hiraki further teaches the dynamic random access memory includes a control circuit to independently (it should be clear the DRAM circuitry that handles the access performs its designed function independently since its own capabilities adequately performs the intended operations) access the non-volatile memory and a circuit to subordinately processing the access (it should be clear that

when the repair program executing on the flash memory reads data from the DRAM, the DRAM must access the flash through its write and output buffers in order to provide the read information to the flash memory, hence “subordinately processing the access"; see col. 16, lines 34-45 and col. 17, lines 9-16;).

Per claim 28, Hiraki further teaches the non-volatile memory includes plural interfaces (there are separate interfaces in Flash 11 for control, address and data, e.g., Address Buffer 11AB, Input Buffer 11IB and Output Buffer 11OB; see Fig. 1, 14, 17 and 20).

Per claim 79, Hiraki further teaches accessing the dynamic randon access memory is from a device outside the memory module (CPU 10, see Fig. 1, 14, 17 and 20; also see col. 10, lines 44-46).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki [US 6,324,103 B2].

Per claim 10, Hiraki fails to teach the static random access memory (SRAM) has a memory size equal to or smaller than 1/1000 of the memory size of the non-volatile memory. However, Hiraki teaches that the SRAM is utilized as a quick access register file (see col. 11, lines 8-10), which implies small memory size for the SRAM. Hiraki further teaches the flash memory stores boot programs, repair information and other data, implying the flash memory's memory size fairly large compared to that of the SRAM, although Hiraki does not teach the flash is 1000 or greater times the size of the SRAM. The specific ratio between the sizes of the two memories would be dependent on the design specification of the article in Hiraki's invention. Therefore, it is clear that Hiraki already teaches the flash memory size is much greater than that of the SRAM, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that making the flash memory 1000 or greater times the size of the SRAM is design specification dependent.

Per claim 15, Hiraki further teaches access to the non-volatile memory and the dynamic random access memory from outside the memory module is made via the dynamic random memory access interface (see Figs 1, 14, 17 and 20, CPU 10's accesses to Flash 11 and DRAM 12 go through Input Buffer 11IB, Output Buffer 11OB, Input Buffer 12IB and Output Buffer 12OB), but fails to teach the DRAM is a synchronous DRAM (SDRAM). However, it is clear to that SDRAMs can run at a higher clock speed than conventional DRAMs and therefore provides lower access latency than convention DRAMs and it would have been obvious to one ordinarily skilled in the

art at the time of the Applicant's invention to use a SDRAM in Hiraki's invention instead of a convention DRAM to reduce access latency.

Per claim 27, Hiraki further teaches the non-volatile memory includes an error detecting and correcting circuit (see col. 21, lines 4-5 and Fig. 14, Repair Address Register 11AR; Flash 11 contains circuitry for sensing defects and repairing the defects) and an address replacement circuit (repairing defects involves replacing the defect in the address where the defect is detected). Hiraki does not specifically teach the non-volatile memory includes a static random access memory, but teaches the Flash Memory 11 contains small fast access memories such as Repair Address Register 11AR, Address Buffer 11AB and Input/Output Buffers (see Fig. 14). Hiraki further teaches that SRAM is utilized as a quick access register file (see col. 11, lines 8-10), which indicates SRAMs are suitable for implementing small and fast access memories. Therefore, it would have been obvious to one ordinarily skilled in the art to implement the registers and/or buffers in Flash Memory 11 using SRAM for realizing small and fast access memories.

6. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki [US 6,324,103 B2] and Tanzawa et al. [6,072,719] (hereinafter "Tanzawa").

Per claims 16 and 17, Hiraki already substantially discloses the claims as set forth above in claim 15 and further teaches the non-volatile memory is a flash memory (see Fig 1, 14, 17 and 20). Hiraki does not teach the flash memory is a NAND flash memory or a AND flash memory. However, Tanzawa teaches the use of both NAND and AND flash memories, which are suited to flash devices requiring high capacity data storage. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use either a NAND flash memory or an AND flash memory in Hiraki's invention to provide large data storage capacity.

Response to Arguments

7. Applicant's arguments with respect to claims 1-10, 12, 14-17, 21, 24, 25, 27, 28 and 79 have been considered but are moot in view of the new ground(s) of rejection. The newly amendment limitations are taught by Hiraki and Tanzawa as set forth above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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27 June 2007

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